REMARKS

Claims 1-21 remain in the application for consideration of the Examiner.

Reconsideration and withdrawal of the outstanding rejections are respectfully requested in light of the following remarks.

Turning now to the art rejections, Claims 1-21 were rejected under 35 U.S.C. § 102(e) as being anticipated by Ranmuthu.

It is respected submitted that Runmuthu does not disclose or suggest the presently claimed invention including the current sensing portion to sense a change in the bias current based on the resistivity change in the various forms in independent Claims 1, 8, and 15.

The Examiner alleges that Ranmuthu discloses a current sensing portion 180 configured to sense a change in bias current; however, the Examiner's attention is directed to column 4, lines 25 of Ranmuthu where the transconductance circuit compares the V_{BIAS} across terminals 187 and 188 with a target voltage such as V_{DAC} output from the VDAC circuit 186.

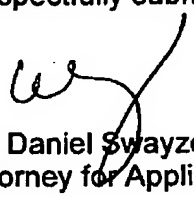
It is clear from this disclosure that the transconductance circuit 182 senses changes in voltage and not current.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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